AN IMPROVED 16 BY 1 ARRAY PHOTON COUNTING FOR SOIL SPECTROSCOPY USING BRENT KUNG ADDER

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ABSTRACT

The traditional process in farming involves many steps of hard labour, which are bush clearing, irrigation and the introduction of manual soil testing. It was evident that the traditional methods of ways of nutrients testing are associated with errors and labour intensive. This paper aim to address the shortcoming by proposing a Field Programmable Gate Array (FPGA) based photon counting system using 16 bits parallel adder (Brent Kung) algorithm to ease the process with the precise result than the conventional. The algorithm used permits parallel computation, high speed and is user friendly on low-cost FPGA module. Verilog hardware description language (HDL) was used on the Vivado suite platform for implementation. The simulation was conducted under different conditions by changing the sample signal with various degrees of frequency. It was found that the proposed FPGA based photon counting system has an improvement in frequency of 46% and reduction of 46% Look-Up Table (LUT), 92% reduction of fan-out over the conventional, which has a frequency of 480 MHz through a tradeoff was seen in the total power.

Keywords: Brent Kung adder, FPGA, high-speed adder, photon counting

1. INTRODUCTION

Farming involves sequences of steps of preparing the land, soil testing and process of planting crops. The soil testing is being carried out basically in two broad categories: the traditional method and by using knowledge of Engineering, such as Verilog Hardware Description Language (VHDL), irrigation and many more agricultural projects are successfully carried out

(Kadu and Rode, 2008). Most soils have a huge amount of nutrients, when soils are repeatedly used for growing and harvesting crops, nutrients level would subsequently decrease in the soil. Low nutrients level in the soil leads to poor growth, vulnerable to diseases and low yield of crops. Therefore, there is a need for soil analysis to determine the nutrients present in the soil, so that the particular mineral(s) that are lacking or inadequate are added to the soil for high crop growth and yield. Even though most soils have a huge amount of nutrients, for a better yield of the crop, there is a need to add the mineral that are lacking by using appropriate fertilizer. Therefore, the farmers must add macronutrients to the soil in the right proportion. Soil macronutrients (nitrogen (N), phosphorous (P) and potassium (K)) are essential nutrients that enhance plant growth hence they are needed in large quantities to enhance plant growth. N aid leaf and stem development and maintain its green colour, P enhances the root system of the crop for better absorption of water and other beneficial nutrients, and K helps the crops in producing flowers and fruits (Mirza, 2018).

To increase crop production, fertilizers containing N, P, and K are crucial. Inappropriate utilization of fertilizers will result in low quality in fruits, vegetables lagging in colour, size, taste and even amount of the fruits. Moreover, the amount of recommended N, P, and K is related to the type of crop and status of plant growth. Also, the amount of fertilizer to be used is further related to the existing substances of N, P, K macronutrients in the soil. Therefore, investigators are looking for ways to enhance plant productivity while reducing fertilizer intake. Soil fertility varied on a small scale all over a cultivated land; several researchers are involved in finding ways of evolving sensors to map these nutrient contents. The spatial and temporal behaviour of N, P, and K is checked by integrated crop management systems that were designed for this purpose. To automate agricultural practice, which will improve crop production, monitoring N, P and K values alongside the ph. should be continued (Shylaja & Veena, 2017).

Furthermore, soil analysis is normally done in the laboratory after the soil sample has taken from the field and the analysis cannot be done immediately. To analyze soil nutrients, specific colours are produced from the reaction of the chemical reagents with the soil sample for a particular nutrient. The degree of the presence of nutrient is measured by comparing against a colour chart since this is done manually, it is very slow to take days to complete the testing, without quantitative values and lead to errors in the report (Adhikary *et al*., 2015; Ingale *et al*., 2016).

Therefore, there is a need to investigate the developed colour solution. A spectrophotometer is applied for this purpose, which is faster. However, the system of the spectrophotometer is complicated, expensive and needs an operator to function properly. The developed of a sensing unit comprises; Light Emitting Diode (LED), photodiode (PD), microcontroller, analog to digital converter (ADC) and general packet radio service (GPRS) modem is reported by Adhikary *et al*. (2015). The PD received the light beam, which passes through the soil sample that is generated from the light source LED; the received light can be used to compute the presence of the nutrients in the sample. The result from the system shows a little deviation of about 5% from the Laboratory result, which is according to the researcher is not costly to compare to the spectrophotometer and does not requires an operator (Adhikary *et al*., 2015).

However, the system is very slow, operates sequentially and requires a network since is GPRS-based which makes it expensive due to data subscription, the colour detected is in form of red, green and blue (RGB) which may not be accurate. To solve this problem, a design was proposed with an architecture of the sensing unit based on the Field Programmable Gate Array (FPGA) system (Ingale *et al*., 2016). The system is a standalone device which has a similar procedure with another proposed system, except for GPRS, and instead of computing RGB values directly, the RGB would be converted to hue (H) intensity (I) saturation (S) values (Adhikary *et al*., 2015). The system gives accurate result compared to that RGB, but does not operate in real-time and process data serially. The macronutrients are the most needed for fertilizer application recommendation, zinc (Zn), magnesium (Mg) and calcium (Ca) are macroelements or macronutrients and are also essential nutrients for plant growth. A solution to this situation was proposed, by developing a program that will indicate or measure soil pH and six different nutrients level. The nutrients to be measured are nitrogen, phosphorous, potassium, zinc, calcium, and magnesium by using image processing and Artificial Neural Network (ANN) on the MATLAB platform. A camera was used to capture the pictures of the sample for each nutrient, the images are processed through MATLAB, and the model for the training was done with ANN. The program implementation was carried out successfully, and a qualitative result was obtained Puno *et al.* (2017).

Moreover, the ANN requires adequate data training to obtain an accurate result, the training process often takes longer time and operate sequentially, since the system was based on a

microcontroller, which slows down the operation. The fertilizer recommendation based on the qualitative result of soil nutrients for specific crops, could lead to under or over-application of the fertilizer. Under the application of fertilizer will lead to plant disorder and over-application also amounts to a waste of resources, which should be discouraged. The processing speed should be enhanced to fast-track the measurement. The measuring should be improved to handle high-speed parallel data computation. Furthermore, research-based on parallel prefix adder (Kogge Stone) processing was designed with 16 signals on Qurtus II platform. The design has high resource utilization with low frequency (Kumar, 2018).

To solve this problem, this research is proposed to develop a parallel processing system that can handle 16 incoming signals from spectroscopy. The 16 signals are represented by digit 0 to 15. To achieve the implementation of the parallel system, an algorithm and platform that can support parallel processing must be adapted. Parallel prefix (Brent Kung) adder algorithm and FPGA respectively are proposed. 16-bit high-speed-processing unit based on FPGA, which is incorporated in spectroscopy.

The spectroscopy system comprises a light source that generates light, which is dispersed through monochrome, the optical fiber was used for propagating the light source to a cuvette containing a solution. The solution would be absorbed some of the light, the absorbance level depends on the concentration of ions in the solution. Also, the unabsorbed light would pass through the solution to the detector where the light energy will be detected and converted to current by a photodetector. The weak current is amplified through an amplifier and converted to a voltage. The analog voltage is converted to a digital voltage by analog to digital converter, which sends the signal to FPGA for processing and counting. The FPGA module consists of a 16-bits buffer that is used to synchronize the unsynchronized incoming signal from spectroscopy, which is asynchronous. The Brent Kung adder is served as the counter of the signals. A clock divider is used to maintain the appropriate timing for the circuit to operate accurately. The PISO is used to convert the parallel signal to serial at the output (Kondamacharyulu *et al*., 2019). Both buffer and PISO are registers, that is, they are synchronous system, the clock divider is used to ascertain the data integrity at the output of the PISO. The objectives of the study are to reduce resource utilization such as look up tables (LUT) and fan-out, improve the frequency of the system.

2. MATERIAL AND METHODS

The designs and simulation were carried out using the Vivado Xilinx software environment, to synthesize and simulate it. After the simulation, the timing, frequency and power consumption will be check to observe that it meets the requirement. If the requirement was not met, then the design needs to be optimized, redesign again, synthesize and simulate. The design was tested several times until the requirements are met and satisfactory. Before then, the individual components of the circuit had been designed separately, synthesize, simulated and tested for the requirement. The design flow is described in Figure 1.

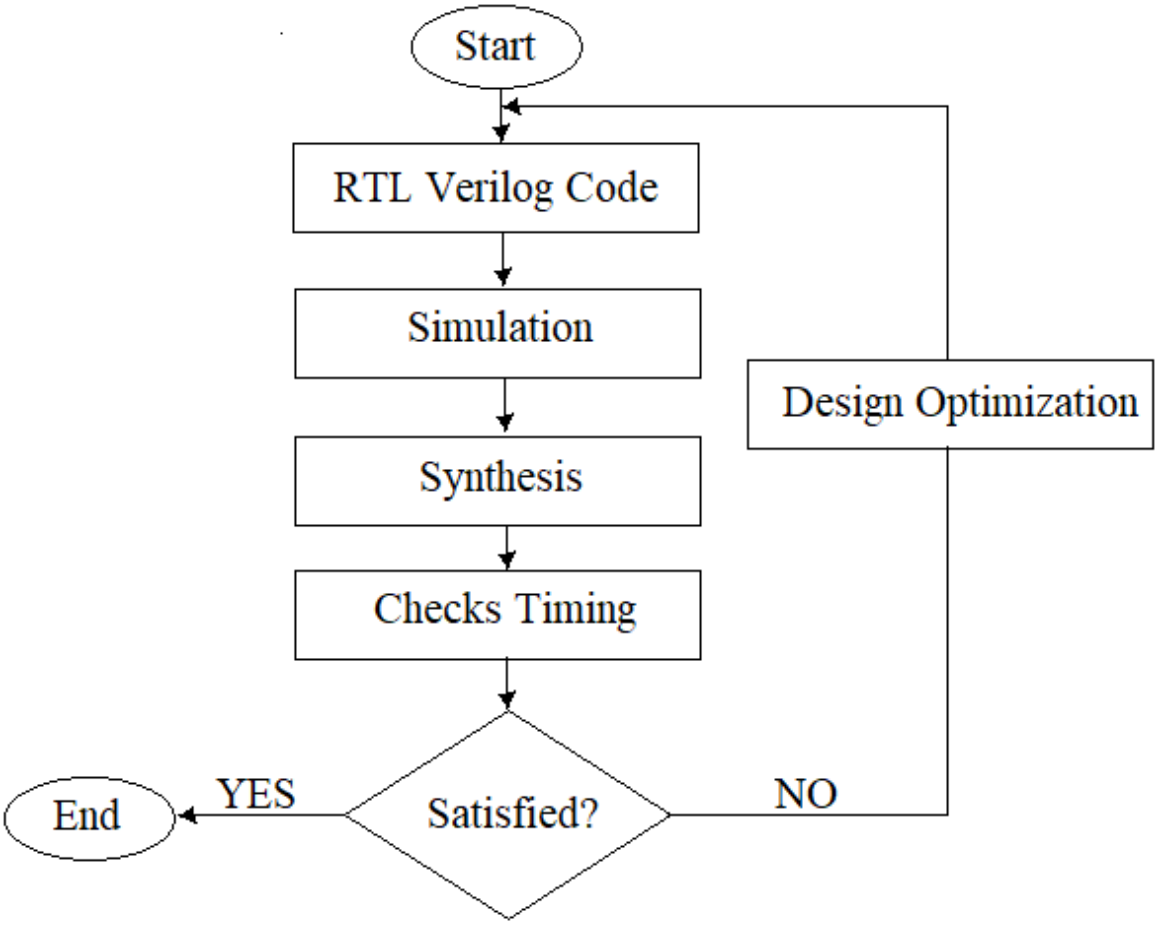

Figure 1: Research flow diagram

2.1 Design of Photon Counting

The complete block diagram of the circuit comprises of a16-bits buffer, 16-bits Brent Kung adder, clock divider, and PISO presented in Figure 2. The circuit comprises the 16-bits buffer

that was used to synchronize the unsynchronized incoming signal from the spectroscopy, which is asynchronous. The Brent Kung adder is served as the counter of the signals. A clock divider is used to maintain the appropriate timing for the circuit to operate correctly. The PISO is used to convert the parallel signal to serial. Both buffer and PISO are registers, that is, they are synchronous system, the clock divider is used to ascertain the data integrity at the output of the PISO. The block diagram of the circuit is presented in Figure 2.

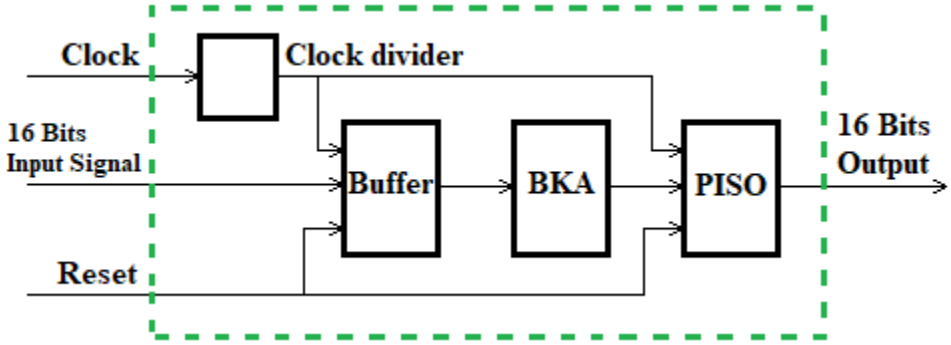

Figure 2: Block diagram of photon counting using FPGA

2.1.1 16-bits buffer RTL circuit

The 16-bits buffer was separately synthesized using Verilog language in Vivado Xilinx to observe its timing, power consumption, and frequency. The buffer has 18 input signal ports and 16 output signal ports. One of the ports is for reset (rst), which reset the buffer to zero by making the reset signal high in this case, Another port is dedicated to clock (clk) is a positive edge clock signal, which synchronizes the input data and output data at the positive edge clock. The remaining 16 port din are inputs of the data ports. The output ports dout are the data output ports of the buffer. The buffer was used to stabilize the inputs signals for proper processing. During the positive clock edge, dout equal to din while din received another signal.

2.1.2 Clock divider RTL circuit

A clock divider is a counter that is generated from a clock. The clock is divided into two clkdv2 and sixteen clkdv16 signals. Because the data from the spectroscopy have to be sample after all the sixteen signals have been shifted out in PISO. The clkdv16 is used to synchronize input

buffer to avoid collision of data or loss of data before the shifting is completed. The normal clock is used in PISO shifting serially. The clock divider was synthesized and simulated in Vivado Xilinx.

2.1.3 Brent Kung adder RTL circuit

The Brent Kung adder consists of a pre-processing step; carry generation step and post-processing step. 16-bits Brent Kung adder, which is used as a counter for photon counting system. The Brent Kung adder is synthesizing using Verilog language in Vivado Xilinx separately to observe its timing, power consumption, and frequency. The Brent Kung adder is generated using the Equations (1)(1) to (7)(Abidin *et al*., 2012).

2.2 Brent Kung Design Steps

The following steps are the steps for the design of Brent Kung.

2.2.1 Preprocessing step

The preprocessing step is the first step of operation in the Brent Kung design, propagate (Pi) and generate (Gi) signal of pairs of A and B signal was carried out using Equation (1) and (2).

$$Gi = Ai.Bi \quad (1)$$

$$Pi = Ai\ xor\ Bi \quad (2)$$

2.2.2 Carry generation step

The carry generation step is the next computation after the pre-processing step. The step is very important because 80% of the Brent Kung design lies in this step, it comprises the black cells, grey cells, and buffer. The black cell has an AND and OR logic gates that give out ($G_{i:j}$) generates and propagates($P_{i:j}$) from previous pre-process with the used Equation (3) and (4).

$$G_{i:j} = G_{i:k} + (P_{i:K}.G_{K-1:j}) \quad (3)$$

$$P_{i:j} = P_{i:k}.P_{k-1:j} \quad (4)$$

The grey cells ($G_{i:j2}$) were generated after the black cells which fed to the post-processing step that leads to the design of the adder. The grey cell was generated using Equation (5).

$$G_{i:j2} = G_{i:k} + (P_{i:K}.G_{K-1:j}) \quad (5)$$

2.2.3 Post-processing step

The post-processing step is the last in the design of the Brent Kung adder, where the final sum (Si) and carry (C_i) was generated using Equations (6) and (7) (Krishna *et al.*, 2018). The adder was designed with Verilog in Vivado Xilinx software environment version 3. Where $i, k, j = (0, 1, 2, 3, \ldots 15)$.

$$C_i = G_i + P_i.C_{i-1} \; or \; C_i = G_i \quad (6)$$

$$Si = P_i xor C_{i-1} \quad (7)$$

After the design and synthesize of the Brent Kung, it was found that the frequency achieved was 385 MHz due to high critical path delay (CPD), which is considered insufficient, since the frequency will be further divided by 16 which is 24 MHz to enable correct sampling. To solve this problem, a two-stage pipeline was introduced to Brent Kung to reduce the CPD. The block diagram of the two-stage pipeline and the RTL schematic of CPD are presented in Figure 3 and Figure 4 respectively.

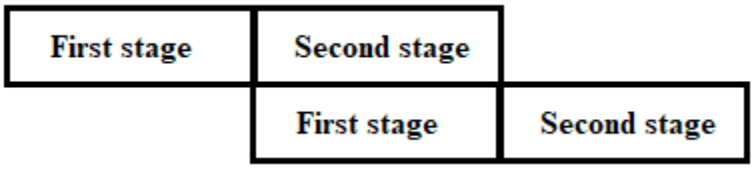

Figure 3: Two-stage pipeline

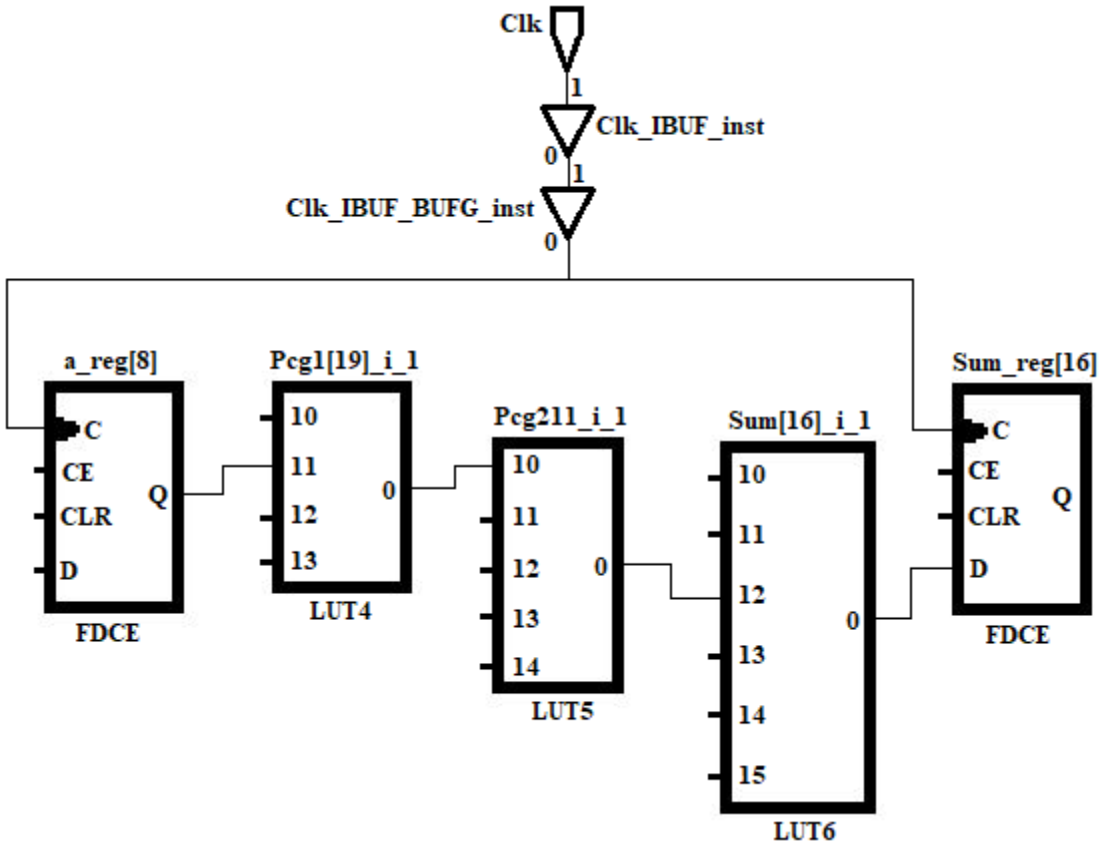

Figure 4: RTL schematic of CPD of Brent Kung adder

2.3 16-Bits PISO Rtl Circuit

The 16 bits PISO has two 16 bits registers, shifter, 16 bits input ports dd, rst, clk, enable en, 16 bits temporary register. The dd received signals from the Brent Kung adder result which was been held in that register. The register was controlled by control enable (CE), which was controlled by en. When the CE is high, the parallel data in the register was passed to the shifter. After shifting, the result is stored in a temporary register, and the least significant bit is generated serially.

Thereafter, the Analysis of sub-system components and the complete system will be presented in the subsequent sections. The sub-system components are 16-bits buffer, clock divider, 16-bits bring Kung adder and PISO. After the schematic diagram was obtained from the model equations, the simulation was carried out and the waveform was generated using Verilog in the Vivado Xilinx environment. From Vivado simulation, Worse Negative slack (WNS) time is

observed and the circuit time was measured using Equation (8) and when the timing report summary was executed. The execution of this timing report summary was conducted after the setting of timing constraint in the Vivado environment for synthesize and implementation which results in WNS (ns) and in turn, used in finding the maximum frequency of the device by using Equation (9). These settings were carried out for the buffer, clock divider, Brent Kung adder, PISO, and the complete integrated device circuit. Furthermore, the power analysis was also carried out using power report analysis in the Vivado environment. The worst-case circuit time and maximum frequency were obtained from the following equation.

Let $T_R$be the required time, $T_C$be circuit time, F_X be maximum frequency and $T_S$be worse negative slack time (Theodore, 2019; Rahman, 2017).

$$T_R - T_C = T_S \;\; \Rightarrow T_C = T_R - T_S \tag{8}$$

$$F_{MAX} = \frac{1}{T_C} \tag{9}$$

where$T_R$the time set by the user is, T_S is worse case time of the device circuit, which can be observed in Vivado. The T_C is the time that the circuit can operate without hitches. The T_C is derived from Equation (8).

2.4 Complete System of Photon Counting

The individual components buffer, clock divider, Brent Kung adder, and PISO were designed successfully, synthesized and simulated in the VivadoHLx 2018-3 edition as illustrated in Figure 5. The functionality was ascertained and then the components were integrated to form a complete system. The complete system was also synthesized and simulated as a whole, the correctness was also confirmed by testing with various timing and inputs. The RTL schematic diagram of the system is presented in Figure 6.

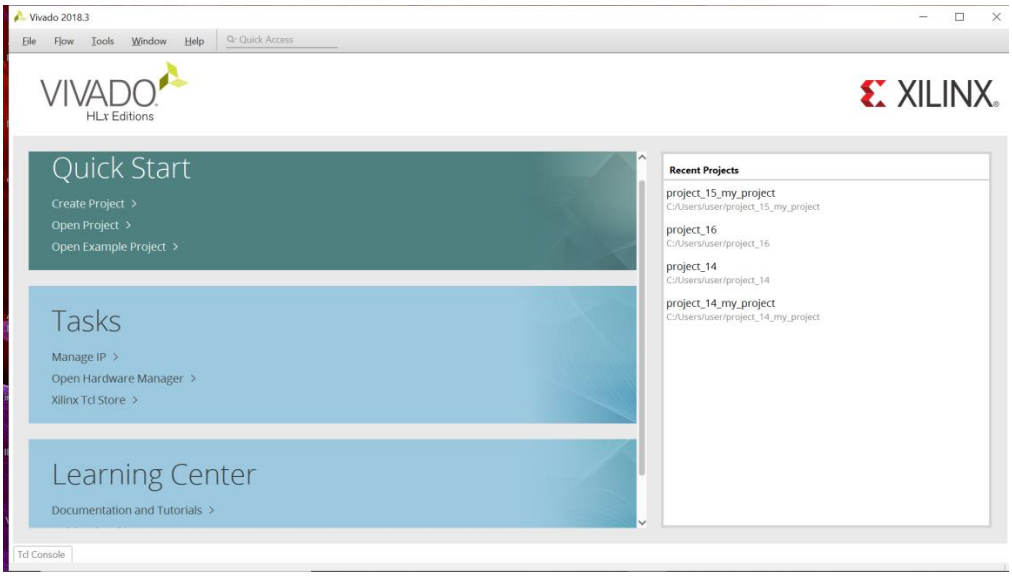

Figure 5: Vivado Xilinx environment

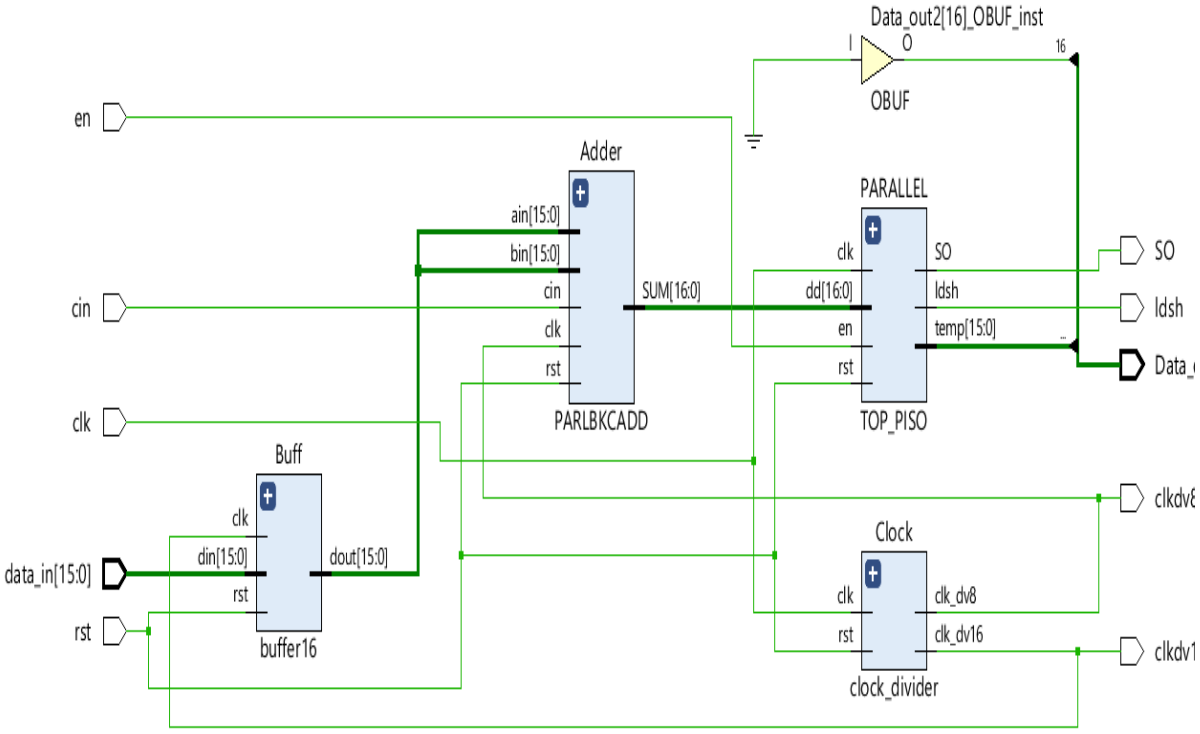

Figure 6: Complete system of the photon counting

3. RESULTS AND DISCUSSIONS

This section presents the results of the design synthesize and simulation obtained and discusses it in detail. The result of resource utilization, frequency, timing and power consumption will be

illustrated.

The components of the photon counting circuit Vivado 2018-3 RTL frequency, resource utilization and power result, comprises16-bits buffer, clock divider, Brent Kung adder, and PISO were designed in the Kintex-7 family of Xilinx in Vivado. The design was synthesized and simulation of post-synthesize was carried out, and the waveform was generated for each component. The analysis of timing, power, and area was also performed.

The design synthesize of the system was successfully carried out in the Vivado suits environment. The simulation of the synthesize was obtained, which shows that the system is functioning correctly. When the rst is HIGH, the content of the buffer and the PISO be cleared, then the rst was set to LOW and en is set HIGH to enable the buffer to load data from input. From the PISO l_{dsh} have to be HIGH to load data from the output of Brent Kung adder. After loading the PISO, l_{dsh} is set to LOW to enable shifting of the loaded data to serial out (SO) of the PISO. From the SO, the data is either "1" or "0" as presented in Figure 7. The parameter of the photon counting system is presented in Table 1.

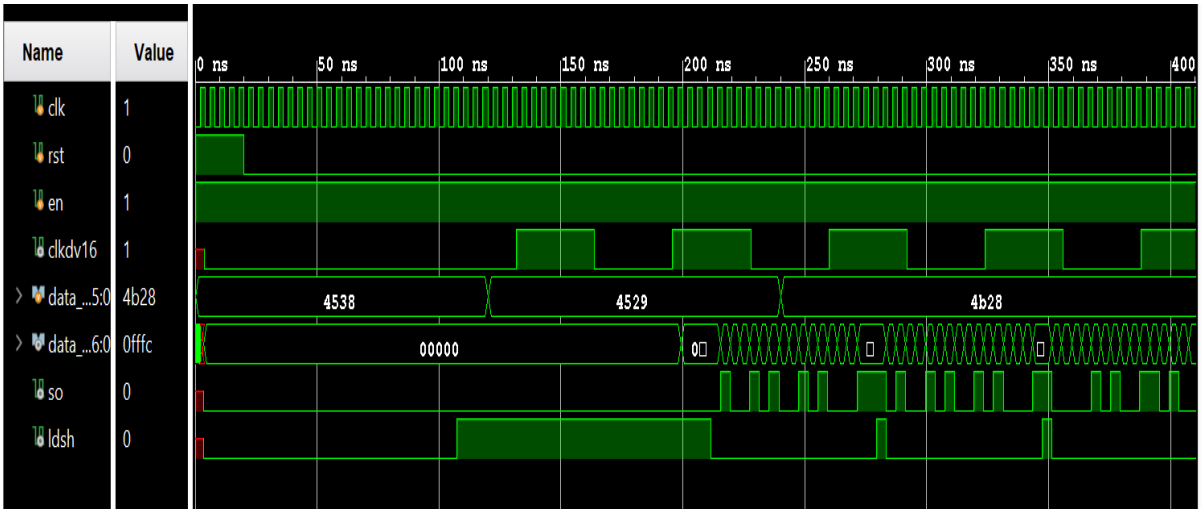

Figure 7: Full system of photon-counting Vivido 2018-3 RTL synthesize result

Table 1: Parameters for photon counting system using Vivado

Name	Period (ns)	WNS (ns)	Frequency (MHz)	F_{MAX} (MHz)	Maximum Power (Mw)
Buffer	1.6	0.775	625	1212.0	114
Clock divider	1.6	0.461	625	878.0	92
PISO	1.6	0.062	625	650.0	134
Brent Kung adder	2.0	0.414	625	630.5	141
Complete system	1.6	0.141	625	685.0	176

In FPGA, the resources available to be used are not in form of logic elements like AND, NAND XOR, NOR gates, rather, they are presented as lookup tables slice memory, flip flops (FF), input and outputs (io), etc. the LUT is where the logic elements will be configured to suit the designer needs. The design utilized 49 LUT and 29 fan-out resources as shown in Figure 8 and presented in Table 2 with an average fan out of 1.933 in the Vivado as presented in Figure 9. The less fan out was also found in the researcher (Taj, 2017). The previous design of Kogge Stone adder (Kumar, 2018) has 89 LUT 343 fan-out and an average fan-out of 2.47.

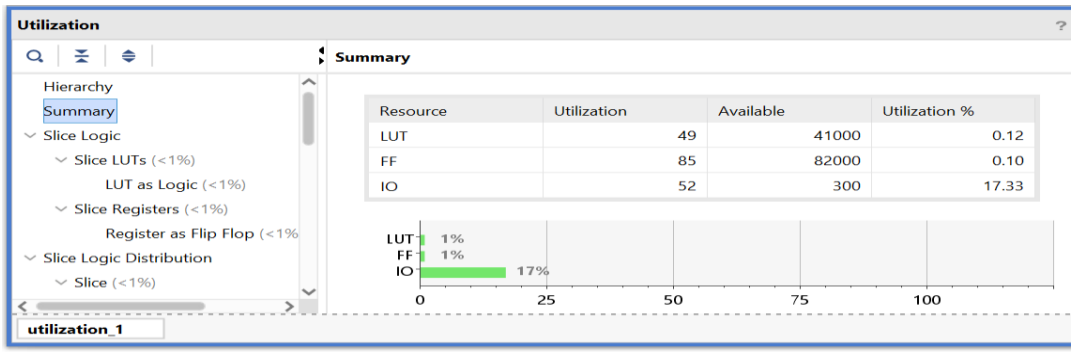

Figure 8: Resources utilization

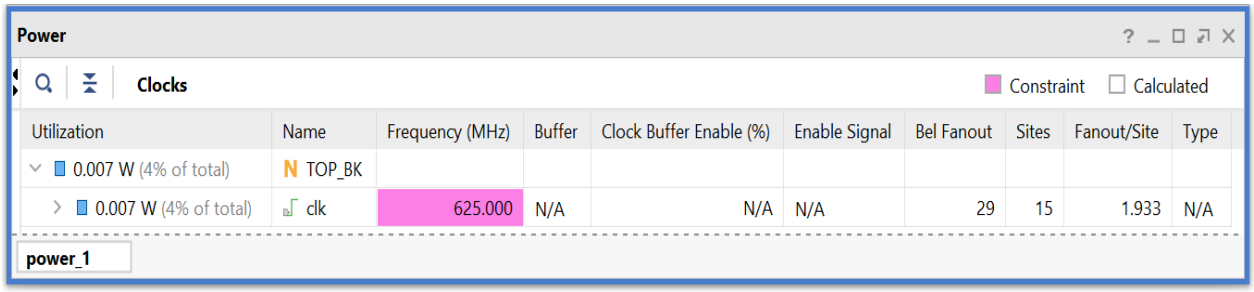

Figure 9: 16-bits photon counting average fan-out

Table 2: Resources utilization

Resources	Used	Available
Look up tables	49	41000
D flip flops	85	82000
Input/outputs	52	300

The design of the Brent Kung system counter in Vivado Xilinx was successfully carried out, the timing, frequency, LUT, and power consumption were measured. Different dead time was applied to design, for each dead time, corresponding values of WNS, power was recorded and presented in Table 3.

Table 3: FPGAphoton counting system parameters

Frequency (MHz)	WNS (ns)	T_C (ns)	Power (W)	WPWS (ns)
100	8.568	1.43	0.14	4.600
200	3.568	1.43	0.147	2.100
300	1.898	1.44	0.154	1.265
400	1.068	1.43	0.161	0.850
500	0.568	1.43	0.168	0.400
600	0.234	1.43	0.175	0.066
700	-0.003	1.43	0.181	-0.171
800	-0.182	1.43	0.188	-0.350
900	-0.322	1.43	0.195	-0.490
1000	-0.432	1.43	0.202	-0.600

From Table 3 values, Figure 10 of WNS versus frequency was plotted to observe the maximum frequency acceptable by the design to function according to specification. Moreover, the design will malfunction, if it operates at a frequency, which, the WNS is less than zero as indicated by the arrow in the figure below. Therefore, the maximum allowable frequency is around 699 MHz at 176 mW. Even though the FPGA Xilinx Kintex 7 series limit toggle rate to 625 MHz. the high frequency and less area observed in the process had been expected based on the reports (Rani, and Kalyani, 2017; Raju *et al*., 2016; Abidin *et al*., 2012; Krishna and Krishna, 2018; Potdukhe and Jaiswal, 2016) which state that, the Brent Kung adder had high frequency and less area.

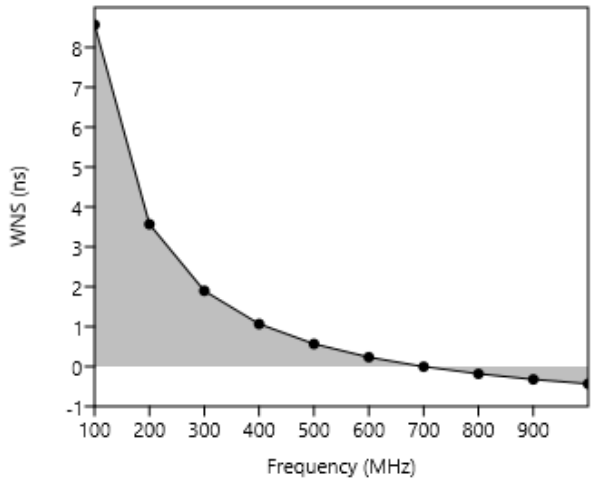

Figure 10: FPGA WNS versus frequency

The power of the design was measured for each of the corresponding frequencies as shown in Table 3. The power was found to have a linear relationship with frequency, as frequency increase, power also increases as illustrated in Figure 11 with the correlation coefficient of $R^2$is 0.99992. This confirms the stand of (Abidin *et al*., 2012; Raju *et al*., 2016; Potdukhe and Jaiswal, 2016; Rani *et al*., 2017; Krishna and Krishna, 2018) which states that Brent Kung adder has high speed and less area than the previous ordinary PPA system.

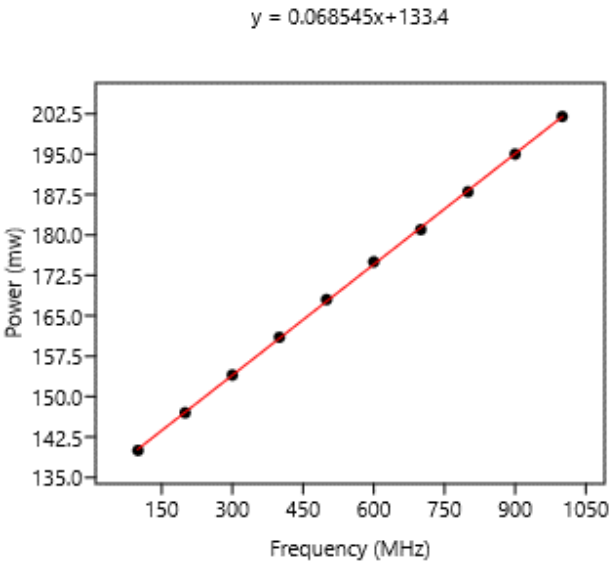

Figure 11: FPGA power versus frequency

The comparison of the proposed design with the previous design in terms of frequency, resource utilization and power was carried out. The result for the resource utilization was presented in

Table 2 with 46% reduction of LUT, 92% reduction of fan-out and 46% improvement of frequency. The tradeoff is certainly unavoidable for any design, the only thing is to minimize the consequences the proposed design can be an exception, with 76% increase of power compared with the previous design (Kumar, 2018) that has a maximum frequency of 480 MHz as shown Figure 12, with the maximum power consumption of 40 mW as illustrated in Figure 13.

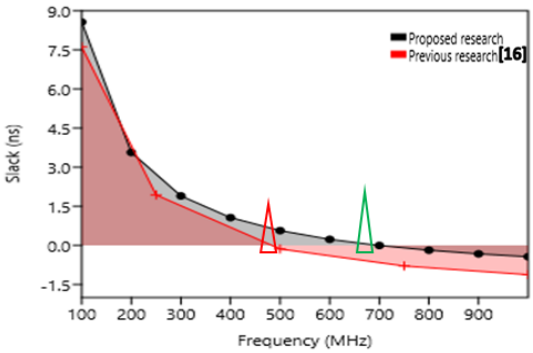

Figure 12: Comparison between the proposed design and the previous one of Slack and frequency

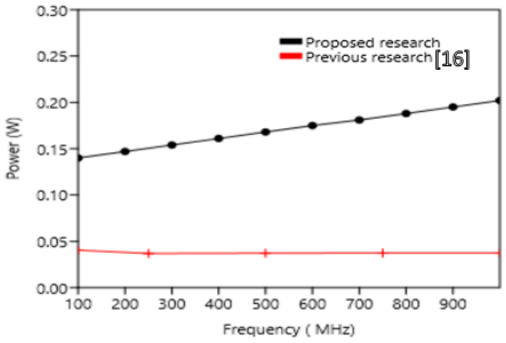

Figure 13: Comparison between the proposed design and the previous one of power and frequency

4. CONCLUSION

The design 16 bits of improved photon counting was successfully synthesized simulated and was carried through the Vivado Xilinx environment based on Brent Kung adder. Furthermore, various slack timing, frequency, power analysis were carried out and benched marked with the previous design which is based on Kogge stone adder quartos II. The design utilized 49 LUT and 29 fan-out resources with an average fan out of 1.933. The design used less LUT of 55% compared to previous research which leads to a decrease of the area and 46% of increased frequency will enhance faster operation which can be utilized for real-time operation with increase power.

5. RECOMMENDATION FOR FURTHER WORK

The design of the photon counting is done in the FPGA based, it can be designed in Application Specific Integrated Circuit (ASIC) to improve the power and area by maintaining or improving the frequency of the design.

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